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ABSTRACT OF THE DISCLOSURE

In order to efficiently process image data in a circuit dividing single image data into a plurality of data and processing the data with a plurality of MPUs in parallel with each other, the MPUs process image data input through an input image data in parallel with each other. An address bus inputs addresses of the image data, and address memories provided on the MPUs store the addresses of the image data processed by the MPUs respectively. When the image data are completely processed, the image data are output through an output image bus while the addresses of the image data are output through the address bus.